REMARKS

Claims 1-46 remain in the application as originally filed.

The specification is amended to correct matters of a typographical nature. In reviewing the application as-filed, the undersigned noted that different components were designated in Figs. 1 and 2 with the same numeral 30. Accordingly, the specification is amended to refer to the sidewall spacers with the numeral 29. Substitute drawings are provided herewith making this numeric change. Acceptance and entry of the substitute drawing sheets bearing Figs. 1 and 2 are hereby requested.

Application appreciates the Examiner's indicated allowability of the subject matter of claims 4, 6-8, 10, 11, 13-21, 24 and 26-46. Claims 1-3, 5, 9, 22, 23 and 25 stand rejected. Applicant disagrees and requests reconsideration.

Of those claims rejected, claims 1, 9, 12 and 22 are independent claims. Each such claim is rejected as being anticipated by one or both of Liaw et al. and McDaniel et al. It is therefore the Examiner's assertion that such references disclose each of the limitations of such independent claims. However, each of Applicant's independent claims 1, 9, 12 and 22 recite "voltage or current controlled resistance setable semiconductive material". Neither Liaw et al. nor McDaniel et al. is interpreted to disclose such material anywhere, let alone in the context of Applicant's claim combinations.

"Resistance setable semiconductive material" is, by definition, a material whose resistance is not inherently constant, and which can be varied and set

(i. ., s Applicant's specification at p.7, lns.18-21, and ar p.11, ln. 11). Furth r, th subject claim limitation requires that such material is capable of being variably set by at least one of voltage and current. Accordingly, the setting of the resistance of such semiconductive material is controlled by the application of at least one of voltage and current. No other reasonable interpretation can be drawn from Applicant's specification and claims as to what "voltage or current controlled resistance setable semiconductive material" means.

With respect to Liaw et al., the Examiner points to Fig. 6 and col.5, lns.33-52. However, Fig. 6 depicts a plug-like contact comprised of a titanium silicide 9; a titanium layer 7a, 7b; a titanium nitride layer 8; another titanium layer 10; and a tungsten layer 11. The overlying line is formed of a metal interconnect structure 12 which is apparently not otherwise defined. Regardless, not one of the disclosed materials is semiconductive. In addition, not one of the disclosed materials can have its resistance varied to different set states after its deposition by any means, let alone be controlled by at least one of voltage or current as Applicant specifically claims. None of the other constructions or materials disclosed in Liaw et al. constitutes a "voltage or current controlled resistance setable semiconductive material" in the context of Applicant's claims. Accordingly, Liaw et al. does not disclose this facet of any of Applicant's independent claims, and therefore, the anticipation rejection

of independent claims 1, 9, 12 and 22 over Liaw et al. should be withdrawn. Action to that end is requested.

The same essential argument applies to McDaniel et al. The Examiner points specifically to Fig. 1 and col.3, lns.54+. However, each of the materials disclosed in McDaniel et al. is understood to be either conductive, semiconductive or insulative. None are disclosed, either expressly or impliedly, as being capable of having their resistance set by any means, let alone by at least one of voltage and current control, as Applicant has claimed. Therefore, Applicant recites in independent claims 1, 9, 12 and 22 something which is not disclosed by McDaniel et al. Accordingly, the anticipation rejection of these independent claims should be withdrawn, and action to that end is requested.

The secondary Chiang et al. reference cited in the rejection of Applicant's dependent claim 5 is likewise seen to be inapplicable in this regard. Further, with respect to this and Applicant's other dependent claims, such should be allowed as depending from allowable base claims, and for their own recited features which are neither shown nor suggested in the cited art. Action to that end is requested.

This application is believed to be in immediate condition for allowance, and action to that end is requested. If the Examiner disagrees with any of the Applicant's assertions above, the Examiner needs to point to specific language in the cited references which disclose or suggest a resistance

setabl s miconductiv material, th resistance of which is controlled by voltag or curr nt. Th undersigned finds no such language.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.	09/921,518
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Inventor	John T. Moore
Assignee	Micron Technology, Inc.
Group Art Unit	2818
Examiner	Phuc T. Dang
Attorney's Docket No.	MI22-1669

Title: Method of Forming Integrated Circuitry, Method of Forming Memory Circuitry, and Method of Forming Non-Volatile Random Access Memory Circuitry

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO MARCH 29, 2002 OFFICE ACTION

In the Specification

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Th last paragraph n pag 7, beginning at lin 22 has been amended as follows:

Fig. 1 depicts but one preferred implementation of the invention in a method of forming non-volatile random access memory circuitry. A plurality of memory cell access transistor gates 14, 16, 18 and 20 are formed over semiconductor substrate 12. By way of example only, such comprise a gate dielectric layer 22, an overlying conductively doped polysilicon layer 24, an overlying conductive metal silicide layer 26, an insulative cap 28, and opposing anisotropically etched insulative sidewall spacers ~~30~~ 29. In the depicted preferred embodiment, gate constructions 14-20 are in the form of memory cell wordlines. Substrate isolation, for example LOCOS field isolation oxide or trench isolation, is not shown for clarity, and as not constituting particular materiality to the invention. Discussion proceeds with processing particularly material to memory cell wordlines 16 and 18 which are proximate one another.

The first complete paragraph on page 7, beginning at line 3 has been amended as follows:

Such provides but a few examples of forming integrated circuitry, such as memory ~~circuitry~~ circuitry, in accordance with but some aspects of the invention, with memory cells 54 and 56 constituting but exemplary memory cell storage devices comprising voltage or current controlled resistance setable semiconductive material. Yet in one aspect, the invention comprises a method of forming any memory circuitry which sequentially comprises the formation of some plurality of metal interconnect lines over a semiconductive substrate followed by the formation of a plurality of memory cell storage devices comprising voltage or current controlled resistance setable semiconductive material. Further considered, the invention comprises any method of forming integrated circuitry (whether existing or yet-to-be-developed) which sequentially comprises forming at least one metal interconnect line over a semiconductive substrate followed by the formation of any device comprising two metal comprising electrodes separated by a voltage or current controlled resistance setable semiconductive material.

Th last paragraph on pag 13, beginning at lin 17 has been am nded as follows:

These and other aspects of the invention are also considered and contemplated by way of example only with respect to but one exemplary alternate embodiment depicted in Figs. 3-8. Fig. 3 depicts a wafer fragment 60 comprising a bulk semiconductive substrate 62 having an exemplary shallow trench field isolation region 64 formed therein. Various exemplary conductive device components 66, 68, 70, 72, 74 and 76 are shown as being formed over substrate 62. Such might constitute completed devices or devices in fabrication in the form of conductive lines, such as interconnect lines or field effect transistor lines, or any other conductive device or component thereof. By way of illustration and example only, such device components are depicted as having conductive polysilicon portions 77, overlying metal portions 79, and insulative silicon nitride caps 78. A dielectric layer 80 has been deposited, and planarized back. An exemplary silicon nitride layer 82 is formed thereover. Exemplary contact openings have been formed through layers 82 and 78 with respect to conductive device ~~component~~ components 66, 68, 70, 74 and 76.

END OF DOCUMENT